IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Theodore W. Houston | Docket No.: TI-35974

Serial No.: 10/732,970 | Confirmation No.: 8532

Filed: 12/11/2003 | Examiner: Phan, Trong Q.

Art Unit: 2827

Title: An SRAM Device and a Method of Operating the Same to Remove Leakage Current during a Sleep Mode

APPEAL BRIEF UNDER 37 CFR §1.192

June 11, 2007

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

Pursuant to the Office Action dated 01/19/2007 and the Notice of Appeal dated 05/18/2007, the Appellants submit this Appellants' Brief. The Commissioner is hereby requested and authorized to charge any fees necessary for the filing of the enclosed papers to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

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REAL PARTY IN INTEREST

The Real Party in Interest in the present appeal is Texas Instruments Incorporated, the assignee, as evidenced by the assignment set forth at Reel 014798, Frame 0460.

RELATED APPEALS AND INTERFERENCES

No related appeals or interferences are known to the Appellants.

STATUS OF CLAIMS

Claims 1-4, 6-16, and 18-31 are the subject of this appeal. Claims 1-4, 6-16, and 18-31 are pending and rejected.

STATUS OF AMENDMENTS

In response to the non-final Office Action dated March 23, 2005, the Appellants submitted an amendment on July 11, 2005. In response to the non-final Office Action dated August 17, 2005, the Appellants submitted an amendment on October 31, 2005. In response to the final Office Action dated December 21, 2005, the Appellants submitted an amendment on March 16, 2006. In response to the Advisory Action dated April 4, 2006, the Appellants filed an RCE on April 19, 2006.

In response to the non-final Office Action dated May 1, 2006, the Appellants submitted an amendment on July 13, 2006. In response to the final Office Action dated September 26, 2006, the Appellants submitted an amendment on November 30, 2006. In response to the Advisory Action dated December 12, 2006, the Appellants filed an RCE on December 22, 2006.

The Appellants did not file any amendment subsequent to the non-final Office Action dated January 19, 2007.

SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent Claim 1 is directed to an SRAM device (paragraphs 0011 and 0020; element 100 of FIG. 1) having an SRAM array (paragraphs 0011 and 0020; element 110 of FIG. 1, FIGS. 4-5) coupled to row peripheral circuitry (paragraphs 0011, 0020, and 0023; element 120 of FIG. 1) by a word line and coupled to column peripheral circuitry (paragraphs 0011, 0020, and 0024; element 130 of FIG. 1, element 200 of FIG. 2) by bit lines. The device also includes a sleep mode voltage controller (paragraphs 0011, 0020, and 0025-0037; element 140 of FIG. 1, element 200 of FIG. 2) configured to provide both an array high supply voltage V_{ADD} that is lower than a high operating voltage V_{DD} and an array low supply voltage V_{ASS} that is higher than a low operating voltage V_{SS} to the SRAM array during a sleep mode (paragraphs 0011, 0026, and 0040). The array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} are provided concurrently and the sleep mode voltage controller provides the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a transistor parameter of at least one transistor of the SRAM array (paragraph 0040).

Claim 2 is dependent on Claim 1 and further specifies that the sleep mode voltage controller provides the array high supply voltage V_{ADD} relative to a well voltage (paragraph 0040).

Claim 3 is dependent on Claim 1 and further specifies that the sleep mode voltage controller provides the array low supply voltage V_{ASS} relative to a substrate voltage (paragraph 0040).

Claim 4 is dependent on Claim 1 and further specifies that the sleep mode voltage controller provides a well voltage at about the high operating voltage V_{DD} during the sleep mode (paragraph 0041).

Claim 6 is dependent on Claim 1 and further specifies that the sleep mode voltage controller adjusts the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a transistor parameter (paragraphs 0029, 0031, 0042).

Claim 7 is dependent on Claim 1 and further specifies that the sleep mode voltage controller employs a component selected from the group consisting of a transistor, a diode, and a low-drop out regulator (paragraphs 0027, 0043).

Claim 8 is dependent on Claim 1 and further specifies that the sleep mode voltage controller further provides a well voltage and the array high supply voltage V_{ADD}, the array low supply voltage V_{ASS} and the well voltage are provided as a set of optimum values for a general technology class of transistors (paragraphs 0013, 0030, and 0041).

Claim 9 is dependent on Claim 1 and further specifies that the sleep mode voltage controller adjusts the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a sleep mode current (paragraphs 0031 and 0042).

Claim 10 is dependent on Claim 9 and further specifies that the sleep mode voltage controller refines the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a diode leakage current (paragraphs 0031 and 0043).

Claim 11 is dependent on Claim 1 and further specifies that the sleep mode voltage controller further provides a well voltage such that an n-channel back bias voltage, a p-channel back bias voltage and a voltage across a SRAM cell are all about a same voltage (paragraph 0030; FIGS. 4-5).

Claim 12 is dependent on Claim 1 and further specifies that the sleep mode voltage controller provides the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a minimum voltage across said SRAM array that is sufficient for data retention (paragraphs 0025 and 0043).

Claim 13 is dependent on Claim 1 and further specifies that the sleep mode voltage controller provides the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a minimum voltage across said SRAM array that is sufficient for data retention and minimizing a total leakage current (paragraphs 0013 and 0027).

Independent Claim 14 is directed to a method of operating an SRAM device (paragraphs 0014 and 0038-0040; element 300 of FIG. 3) involving employing in an integrated circuit an SRAM array (paragraphs 0014 and 0039; element 310 of FIG. 3) coupled to row peripheral circuitry (paragraphs 0014 and 0039) by a word line and coupled to column peripheral circuitry (paragraphs 0014 and 0039) by bit lines. The method also includes providing both an array high supply voltage V_{ADD} that is lower than a high operating voltage V_{DD} and an array low supply voltage V_{ASS} that is higher than a low operating voltage V_{SS} to the SRAM array during a sleep mode (paragraphs 0014 and 0040; element 320 of FIG. 3). The array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} are provided concurrently and the providing the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} is based on a transistor parameter of at least one transistor of the SRAM array (paragraph 0040).

Claim 15 is dependent on Claim 14 and further specifies that providing the array high supply voltage V_{ADD} is relative to a well voltage (paragraph 0040).

Claim 16 is dependent on Claim 14 and further specifies providing a well voltage at about the high operating voltage V_{DD} during the sleep mode (paragraph 0041).

Claim 18 is dependent on Claim 14 and further specifies adjusting the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a transistor parameter (paragraphs 0029, 0031, and 0042; element 330 of FIG. 3).

Claim 19 is dependent on Claim 14 and further specifies that the providing employs a component selected from the group consisting of a transistor, a diode, and a low-drop out regulator (paragraph 0043).

Claim 20 is dependent on Claim 14 and further specifies providing a well voltage and the array high supply voltage V_{ADD}, the array low supply voltage V_{ASS} and the well voltage are provided as a set of optimum values for a general technology class of transistors (paragraphs 0013 and 0041).

Claim 21 is dependent on Claim 14 and further specifies adjusting the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a sleep mode current (paragraphs 0031 and 0042; element 330 of FIG. 3).

Claim 22 is dependent on Claim 21 and further specifies refining the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a diode leakage current (paragraphs 0031 and 0043; element 340 of FIG. 3).

Claim 23 is dependent on Claim 14 and further specifies providing a well voltage such that an n-channel back bias voltage, a p-channel back bias voltage and a voltage across a SRAM cell are all about a same voltage (paragraph 0030).

Independent Claim 24 is directed to an SRAM device (paragraphs 0012 and 0020; element 100 of FIG. 1) having an SRAM array (paragraphs 0012 and 0020; element 110 of FIG. 1, FIGS. 4-5) coupled to row peripheral circuitry (paragraphs 0012, 0020, and 0023; element 120 of FIG. 1) by a word line and coupled to column peripheral circuitry (paragraphs 0012, 0020, and 0024; element 130 of FIG. 1, element 200 of FIG. 2) by bit lines. The device also includes a sleep mode voltage controller (paragraphs 0012, 0020, and 0025-0037; element 140 of FIG. 1, element 200 of FIG. 2) configured to provide both an array high supply voltage V_{ADD} and an array low supply voltage V_{ASS} to the SRAM array during a sleep mode (paragraphs 0012, 0026, and 0040) and modify the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} during transition from an active mode to the sleep mode (paragraph 0012 and 0025). The array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} are provided concurrently and the sleep mode voltage controller provides the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a transistor parameter of at least one transistor of the SRAM array (paragraph 0040).

Claim 25 is dependent on Claim 24 and further specifies that the sleep mode voltage controller performs the modify based on reducing current leakage of the SRAM array and providing sufficient voltage across the SRAM array via the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} to retain data (paragraphs 0025 and 0043).

Claim 26 is dependent on Claim 24 and further specifies that the sleep mode voltage controller provides the array high supply voltage V_{ADD} lower than $V_{n\text{-}well}$ during the sleep mode (paragraph 0025).

Claim 27 is dependent on Claim 24 and further specifies that the sleep mode voltage controller provides the array low supply voltage V_{ASS} higher than a substrate voltage during the sleep mode (paragraph 0025).

Claim 28 is dependent on Claim 24 and further specifies that the sleep mode voltage controller is configured to regulate the array high supply voltage V_{ADD} relative to the array low supply voltage V_{ASS} during the sleep mode (paragraph 0025).

Claim 29 is dependent on Claim 24 and further specifies that the sleep mode voltage controller is configured to regulate the array low supply voltage V_{ASS} relative to the array high supply voltage V_{ADD} during the sleep mode (paragraph 0025).

Independent Claim 30 is directed to an SRAM device (paragraphs 0011 and 0020; element 100 of FIG. 1) having an SRAM array (paragraphs 0011 and 0020; element 110 of FIG. 1, FIGS. 4-5) coupled to row peripheral circuitry (paragraphs 0011, 0020, and 0023; element 120 of FIG. 1) by a word line and coupled to column peripheral circuitry (paragraphs 0011, 0020, and 0024; element 130 of FIG. 1, element 200 of FIG. 2) by bit lines. The device also includes a sleep mode voltage controller (paragraphs 0011, 0020, and 0025-0037; element 140 of FIG. 1, element 200 of FIG. 2) configured to provide both an array high supply voltage V_{ADD} that is lower than a high operating voltage V_{DD} and an array low supply voltage V_{ASS} that is higher than a low operating voltage V_{SS} to the SRAM array during a sleep mode (paragraphs 0011, 0026, and 0040). The array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} are provided concurrently (paragraph 0040).

Claim 31 is dependent on Claim 31 and further specifies that the sleep mode voltage controller further provides a well voltage and the array high supply voltage V_{ADD}, the array low supply voltage V_{ASS} and the well voltage are provided as a set of optimum values for a general technology class of transistors (paragraphs 0013, 0030, and 0041).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-4, 6-16, and 18-31 stand rejected under 35 U.S.C. §102(e) as being unpatentable over the patent granted to Deng et al. (U.S. Pat. No. 6,925,025).

ARGUMENT

1. Rejection under 35 U.S.C. §102(a) over the patent granted to Deng et al. (U.S. Pat. No. 6,925,025).

Claim 1

Independent Claim 1 positively recites that the sleep mode voltage controller provides the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a transistor parameter of at least one transistor of the SRAM array. These advantageously claimed features are not taught or suggested by the patent granted to Deng et al.

Deng et al. teaches away from the advantageously claimed invention because Deng et al. teaches regulating a high operating voltage V_{DDM} and a low operating voltage V_{SSM} to the SRAM array (column 5 lines 60-63); but Deng et al. does not teach providing an array high supply voltage and an array low supply voltage to the SRAM array, as advantageously claimed. The Appellant respectfully submits that the Office Action arguments incorrectly confuse the array high voltage supply (V_{DDA}) of Deng et al. with the high operating voltage (V_{DDM}) of Deng et al. Similarly, the Office Action arguments incorrectly confuse the array low voltage supply (V_{SSA}) of Deng et al. with the low

operating voltage (V_{SSM}) of Deng et al. The Appellant notes that the array high voltage supply is V_{DDA} and the array low supply voltage is V_{SSA} in Deng et al. (column 2 lines 48-55). Therefore, the discussion in the Office Action (pages 2-3) directed to V_{DDM} and V_{SSM} is unrelated to the array high supply voltage and the array low supply voltage (that is the subject of the Appellant's claim). (The Appellant also notes that the array high supply voltage in the Appellants application is labeled V_{ADD} while the array high voltage supply is labeled V_{DDA} in Deng et al. Similarly, the array low supply voltage in the Appellants application is labeled V_{ASS} while the array low voltage supply is labeled V_{SSA} in Deng et al.)

The Appellant also respectfully traverses the statements in the Office Action (page 2) that the inherent "voltage drop across the header-diode" and the inherent "voltage drop across the footer-diode" are the advantageously claimed transistor parameter. The Applicant submits that the inherent voltage drop of an SRAM transistor is an inherent response to the transistor parameter, but it is not the transistor parameter. The Applicant notes that the definition of the term "transistor parameter" is defined in the Specification (paragraphs 0029, 0030, 0031, 0037). Moreover, a statement that "the current leakage is often primarily based on the parameters of the SRAM cell transistors" (page 3 of the Office Action) is not equivalent to the claimed sleep mode voltage controller providing the array high supply voltage and array low supply voltage based on a transistor parameter.

Therefore, Claim 1 is patentable over the patent granted to Deng et al.

Claim 2

Claim 2 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 2 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 1, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 2 further specifies the additional limitation that the sleep mode voltage controller provides the array high supply voltage V_{ADD} relative to a well voltage.

Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach that the array high supply voltage V_{DDA} follows the changes in the well voltage (column 2 lines 48-53). Rather, if the well voltage of Deng et al. deviates from 1.2 volts then V_{DDM} and V_{SSM} will not follow that change (column 6 lines 31-34; FIG. 1). Moreover, the Appellant notes that V_{DDM} (cited in the Office Action) is not the array high supply voltage V_{DDA} of Deng et al. (column 2 lines 48-52). Therefore, the arguments on page 3 of the Office Action are not relevant to the claimed language of Claim 2 (e.g. the “array high supply voltage”).

Therefore, Claim 2 is patentable over the patent granted to Deng et al.

Claim 3

Claim 3 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 3 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 1, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 3 further specifies the additional limitation that the sleep mode voltage controller provides the array low supply voltage V_{ASS} relative to a substrate voltage.

The Office Action (page 3) is silent as to where Deng et al. teaches that the sleep mode voltage controller provides the array low supply voltage V_{ASS} relative to a substrate voltage. Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach that the array low supply voltage V_{SSA} follows the changes in the substrate voltage (column 2 lines 48-53; FIG. 1). Rather, if the substrate voltage of Deng et al. changes then neither V_{DDM} nor V_{SSM} will follow that change (column 6 lines 31-34). Moreover, the Appellant notes that V_{SSM} (cited in the Office Action) is not the array low supply voltage V_{SSA} of Deng et al. (column 2 lines 48-52). Therefore, the arguments on page 3 of the Office Action are not relevant to the claimed language of Claim 3 (e.g. the “array low supply voltage”).

Therefore, Claim 3 is patentable over the patent granted to Deng et al.

Claim 4

Claim 4 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 4 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 1, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 4 further specifies the additional limitation that the sleep mode voltage controller provides a well voltage at about the high operating voltage V_{DD} during the sleep mode.

The Appellant respectfully traverses the statement in the Office Action (page 3) that Deng et al. teaches "the n-well voltage at about high operating voltage VDD" in column 6. Rather, Deng et al. teaches an n-well voltage at "V_{DD} minus the voltage drop" (column 6 lines 18-34). Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach that the sleep mode voltage controller provides a well voltage at about the high operating voltage V_{DD} during the sleep mode (column 6 lines 18-34; FIG. 1).

Therefore, Claim 4 is patentable over the patent granted to Deng et al.

Claim 6

Claim 6 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 6 is allowable on its own merits because it

recites additional features of the invention that, in combination with the limitation of Claim 1, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 6 further specifies the additional limitation that the sleep mode voltage controller adjusts the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a transistor parameter.

Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach that a sleep mode voltage controller adjusts the array high supply voltage V_{DDA} and the array low supply voltage V_{SSA} (column 2 lines 48-53). As stated supra, the Appellant notes that V_{DDM} (cited in the Office Action) is not the array high supply voltage V_{DDA} plus V_{SSM} (cited in the Office Action) is not the array low supply voltage V_{SSA} in Deng et al. (column 2 lines 48-52).

Therefore, Claim 6 is patentable over the patent granted to Deng et al.

Claim 7

Claim 7 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 7 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 1, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 7 further specifies the additional limitation that the sleep mode voltage controller employs a

component selected from the group consisting of a transistor, a diode, and a low-drop out regulator.

The Office Action is silent as to the location of this teaching in Deng et al. The Appellant submits that Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach that a sleep mode voltage controller employs a transistor, a diode, or a low-drop out regulator to provide an array high side voltage and an array low side voltage to the SRAM array (column 2 lines 48-53).

Therefore, Claim 7 is patentable over the patent granted to Deng et al.

Claim 8

Claim 8 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 8 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 1, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 8 further specifies the additional limitation that the sleep mode voltage controller further provides a well voltage and the array high supply voltage V_{ADD}, the array low supply voltage V_{ASS} and the well voltage are provided as a set of optimum values for a general technology class of transistors.

Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach that a sleep mode voltage controller provides an array high side voltage and an array low side voltage to the SRAM array (column 2 lines 48-53). Rather, Deng et al. teaches that the power-down voltage controller provides a high operating voltage V_{DDM} and a low operating voltage V_{SSM} to the SRAM array (column 5 lines 58-63, column 6 lines 14-34). The Appellant notes that V_{DDM} (cited in the Office Action) is not the array high supply voltage V_{DDA} plus V_{SSM} (cited in the Office Action) is not the array low supply voltage V_{SSA} in Deng et al. (column 2 lines 48-52).

Therefore, Claim 8 is patentable over the patent granted to Deng et al.

Claim 9

Claim 9 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 9 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 1, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 9 further specifies the additional limitation that the sleep mode voltage controller adjusts the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a sleep mode current.

The Office Action is silent as to where Deng et al. teaches that the sleep mode voltage controller adjusts the array high supply voltage V_{ADD} and the array low supply

voltage V_{ASS} based on a sleep mode current. Therefore, the USPTO burden under 37 C.F.R. §1.104(c) has not been met. Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach that a sleep mode voltage controller adjusts the array high supply voltage V_{DDA} and the array low supply voltage V_{SSA} based on a sleep mode current (column 2 lines 48-53).

Therefore, Claim 9 is patentable over the patent granted to Deng et al.

Claim 10

Claim 10 is dependent on Claim 9 and is therefore allowable for the same reasons that Claims 1 and 9 are allowable. Furthermore, Claim 10 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claims 1 and 9, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 10 further specifies the additional limitation that the sleep mode voltage controller refines the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a diode leakage current.

The Office Action is silent as to where Deng et al. teaches that the sleep mode voltage controller refines the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a diode leakage current. Therefore, the USPTO burden under 37 C.F.R. §1.104(c) has not been met. Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach that a sleep mode voltage

controller refines the array high supply voltage V_{DDA} and the array low supply voltage V_{SSA} based on a diode leakage current (column 2 lines 48-53).

Therefore, Claim 10 is patentable over the patent granted to Deng et al.

Claim 11

Claim 11 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 11 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 1, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 11 further specifies the additional limitation that the sleep mode voltage controller further provides a well voltage such that an n-channel back bias voltage, a p-channel back bias voltage and a voltage across a SRAM cell are all about a same voltage.

Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach that a sleep mode voltage controller provides a well voltage such that an n-channel back bias voltage, a p-channel back bias voltage and a voltage across a SRAM cell are all about a same voltage (column 6 lines 16-34). The Appellant respectfully traverses the statement in the Office Action (pages 3-4) that in column 6 lines 28-31 Deng et al. teaches "the SRAM array may have about 0.3 volts back bias on both n-channel and the p-channel transistors in addition to about the same voltage of 0.3 volts across the SRAM cell". The Appellant submits that when V_{DDM} is 0.9 volts and

V_{SSM} is 0.3 volts that the voltage across the SRAM cell is 0.6 volts – not 0.3 volts. Therefore, Deng et al. does not teach that an n-channel back bias voltage, a p-channel back bias voltage, and a voltage across a SRAM cell are all about a same voltage.

Therefore, Claim 11 is patentable over the patent granted to Deng et al.

Claim 12

Claim 12 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 12 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 1, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 12 further specifies the additional limitation that the sleep mode voltage controller provides the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a minimum voltage across the SRAM array that is sufficient for data retention.

Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach that a sleep mode voltage controller provides the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a minimum voltage across the SRAM array that is sufficient for data retention (column 2 lines 48-55). The Appellant respectfully traverses the statement in the Office Action (page 4) that in column 2 lines 24-31 Deng et al. teaches the limitations of Claim 12. Rather, Deng et al. states that an apparatus may "enter the sleep mode while still supplying sufficient

voltage across the memory array to retain data", but does not teach that the sleep mode voltage controller has any involvement in data retention (column 2 lines 30-31).

Therefore, Claim 12 is patentable over the patent granted to Deng et al.

Claim 13

Claim 13 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 13 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 1, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 13 further specifies the additional limitation that the sleep mode voltage controller provides the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a minimum voltage across the SRAM array that is sufficient for data retention and minimizing a total leakage current.

Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach that a sleep mode voltage controller provides the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a minimum voltage across the SRAM array that is sufficient for data retention and minimizing a total leakage current (column 2 lines 48-55). The Appellant respectfully traverses the statement in the Office Action (page 4) that in column 2 lines 24-31 Deng et al. teaches the limitations of Claim 13. Rather, Deng et al. states that an apparatus may "enter the

sleep mode while still supplying sufficient voltage across the memory array to retain data", but does not teach that the sleep mode voltage controller has any involvement in data retention and minimizing leakage current (column 2 lines 30-31).

Therefore, Claim 13 is patentable over the patent granted to Deng et al.

Claim 14

Independent Claim 14 positively recites providing the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a transistor parameter of at least one transistor of the SRAM array. These advantageously claimed features are not taught or suggested by the patent granted to Deng et al.

Deng et al. teaches away from the advantageously claimed invention because Deng et al. teaches regulating a high operating voltage V_{DDM} and a low operating voltage V_{SSM} to the SRAM array (column 5 lines 60-63); but Deng et al. does not teach providing an array high supply voltage and an array low supply voltage to the SRAM array, as advantageously claimed. The Appellant respectfully submits that the Office Action arguments incorrectly confuse the array high voltage supply (V_{DDA}) of Deng et al. with the high operating voltage (V_{DDM}) of Deng et al. Similarly, the Office Action arguments incorrectly confuse the array low voltage supply (V_{SSA}) of Deng et al. with the low operating voltage (V_{SSM}) of Deng et al. The Appellant notes that the array high voltage supply is V_{DDA} and the array low supply voltage is V_{SSA} in Deng et al. (column 2 lines 48-

55). Therefore, the discussion in the Office Action (pages 2-3) directed to V_{DDM} and V_{SSM} is unrelated to the array high supply voltage and the array low supply voltage (that is the subject of the Appellant's claim).

The Appellant also respectfully traverses the statements in the Office Action (page 2) that the inherent "voltage drop across the header-diode" and the inherent "voltage drop across the footer-diode" are the advantageously claimed transistor parameter. The Applicant submits that the inherent voltage drop of an SRAM transistor is an inherent response to the transistor parameter, but it is not the transistor parameter. The Applicant notes that the definition of the term "transistor parameter" is defined in the Specification (paragraphs 0029, 0030, 0031, 0037). Moreover, a statement that "the current leakage is often primarily based on the parameters of the SRAM cell transistors" (page 3 of the Office Action) is not equivalent to the claimed providing the array high supply voltage and array low supply voltage based on a transistor parameter.

Therefore, Claim 14 is patentable over the patent granted to Deng et al.

Claim 15

Claim 15 is dependent on Claim 14, and is therefore allowable for the same reasons that Claim 14 is allowable. Furthermore, Claim 15 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 14, is not taught nor suggested by the patent granted to Deng et al. Namely, Claim 15

further specifies the additional limitation that providing the array high supply voltage V_{ADD} is relative to a well voltage.

The Office Action does not contain any discussion regarding the rejection of Claim 15. Therefore, the USPTO burden under 37 C.F.R. §1.104(c) has not been met. Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach that the array high supply voltage V_{DDA} follows the changes in the well voltage (column 2 lines 48-53). Rather, if the well voltage of Deng et al. deviates from 1.2 volts then V_{DDM} and V_{SSM} will not follow that change (column 6 lines 31-34; FIG. 1).

Therefore, Claim 15 is patentable over the patent granted to Deng et al.

Claim 16

Claim 16 is dependent on Claim 14 and is therefore allowable for the same reasons that Claim 14 is allowable. Furthermore, Claim 16 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 14, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 16 further specifies the additional limitation of providing a well voltage at about the high operating voltage V_{DD} during the sleep mode.

The Office Action does not contain any discussion regarding the rejection of Claim 16. Therefore, the USPTO burden under 37 C.F.R. §1.104(c) has not been met.

Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach providing a well voltage at about the high operating voltage V_{DD} during the sleep mode (column 6 lines 18-34; FIG. 1).

Therefore, Claim 16 is patentable over the patent granted to Deng et al.

Claim 18

Claim 18 is dependent on Claim 14 and is therefore allowable for the same reasons that Claim 14 is allowable. Furthermore, Claim 18 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 14, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 18 further specifies the additional limitation of adjusting the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a transistor parameter.

Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach adjusting the array high supply voltage V_{DDA} and the array low supply voltage V_{SSA} (column 2 lines 48-53). As stated supra, the Appellant notes that V_{DDM} (cited in the Office Action) is not the array high supply voltage V_{DDA} plus V_{SSM} (cited in the Office Action) is not the array low supply voltage V_{SSA} in Deng et al. (column 2 lines 48-52).

Therefore, Claim 18 is patentable over the patent granted to Deng et al.

Claim 19

Claim 19 is dependent on Claim 14 and is therefore allowable for the same reasons that Claim 14 is allowable. Furthermore, Claim 19 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 14, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 19 further specifies the additional limitation that the providing employs a component selected from the group consisting of a transistor, a diode, and a low-drop out regulator.

The Office Action is silent as to the location of this teaching in Deng et al. The Appellant submits that Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach that a transistor, a diode, or a low-drop out regulator is employed to provide an array high side voltage and an array low side voltage to the SRAM array (column 2 lines 48-53).

Therefore, Claim 19 is patentable over the patent granted to Deng et al.

Claim 20

Claim 20 is dependent on Claim 14 and is therefore allowable for the same reasons that Claim 14 is allowable. Furthermore, Claim 20 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim

14, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 20 further specifies the additional limitation of providing a well voltage where the array high supply voltage V_{ADD}, the array low supply voltage V_{ASS} and the well voltage are provided as a set of optimum values for a general technology class of transistors.

The Office Action does not contain any discussion regarding the rejection of Claim 20. Therefore, the USPTO burden under 37 C.F.R. §1.104(c) has not been met. Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach providing an array high side voltage and an array low side voltage to the SRAM array (column 2 lines 48-53). Rather, Deng et al. teaches that the power-down voltage controller provides a high operating voltage V_{DDM} and a low operating voltage V_{SSM} to the SRAM array (column 5 lines 58-63, column 6 lines 14-34).

Therefore, Claim 20 is patentable over the patent granted to Deng et al.

Claim 21

Claim 21 is dependent on Claim 14 and is therefore allowable for the same reasons that Claim 14 is allowable. Furthermore, Claim 21 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 14, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 21

further specifies the additional limitation of adjusting the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a sleep mode current.

The Office Action is silent as to where Deng et al. teaches that adjusting the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} is based on a sleep mode current. Therefore, the USPTO burden under 37 C.F.R. §1.104(c) has not been met. Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach adjusting the array high supply voltage V_{DDA} and the array low supply voltage V_{SSA} based on a sleep mode current (column 2 lines 48-53).

Therefore, Claim 21 is patentable over the patent granted to Deng et al.

Claim 22

Claim 22 is dependent on Claim 21, and is therefore allowable for the same reasons that Claims 14 and 21 are allowable. Furthermore, Claim 22 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claims 14 and 21, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 22 further specifies the additional limitation of refining the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a diode leakage current.

The Office Action is silent as to where Deng et al. teaches refining the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a diode leakage

current. Therefore, the USPTO burden under 37 C.F.R. §1.104(c) has not been met. Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach refining the array high supply voltage V_{DDA} and the array low supply voltage V_{SSA} based on a diode leakage current (column 2 lines 48-53).

Therefore, Claim 22 is patentable over the patent granted to Deng et al.

Claim 23

Claim 23 is dependent on Claim 14 and is therefore allowable for the same reasons that Claim 14 is allowable. Furthermore, Claim 23 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 14, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 23 further specifies the additional limitation of providing a well voltage such that an n-channel back bias voltage, a p-channel back bias voltage and a voltage across a SRAM cell are all about a same voltage.

Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach providing a well voltage such that an n-channel back bias voltage, a p-channel back bias voltage and a voltage across a SRAM cell are all about a same voltage (column 6 lines 16-34). The Appellant respectfully traverses the statement in the Office Action (pages 3-4) that in column 6 lines 28-31 Deng et al. teaches “the SRAM array may have about 0.3 volts back bias on both n-channel and the p-channel

transistors in addition to about the same voltage of 0.3 volts across the SRAM cell". The Appellant submits that when V_{DDM} is 0.9 volts and V_{SSM} is 0.3 volts that the voltage across the SRAM cell is 0.6 volts – not 0.3 volts. Therefore, Deng et al. does not teach that an n-channel back bias voltage, a p-channel back bias voltage, and a voltage across a SRAM cell are all about a same voltage.

Therefore, Claim 23 is patentable over the patent granted to Deng et al.

Claim 24

Independent Claim 24 positively recites that the sleep mode voltage controller provides the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a transistor parameter of at least one transistor of the SRAM array. Claim 24 also positively recites modifying the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} during transition from an active mode to the sleep mode. These advantageously claimed features are not taught or suggested by the patent granted to Deng et al.

The Office Action is silent as to where Deng et al. teaches modifying the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} during transition from an active mode to the sleep mode. Therefore, the USPTO burden under 37 C.F.R. §1.104(c) has not been met. Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach modifying the array high supply voltage

V_{ADD} and the array low supply voltage V_{ASS} during transition from an active mode to the sleep mode (column 2 lines 48-53; FIG. 1).

Deng et al. also teaches away from the advantageously claimed invention because Deng et al. teaches regulating a high operating voltage V_{DDM} and a low operating voltage V_{SSM} to the SRAM array (column 5 lines 60-63); but Deng et al. does not teach providing an array high supply voltage and an array low supply voltage to the SRAM array, as advantageously claimed. The Appellant respectfully submits that the Office Action arguments incorrectly confuse the array high voltage supply (V_{DDA}) of Deng et al. with the high operating voltage (V_{DDM}) of Deng et al. Similarly, the Office Action arguments incorrectly confuse the array low voltage supply (V_{SSA}) of Deng et al. with the low operating voltage (V_{SSM}) of Deng et al. The Appellant notes that the array high voltage supply is V_{DDA} and the array low supply voltage is V_{SSA} in Deng et al. (column 2 lines 48-55). Therefore, the discussion in the Office Action (pages 2-3) directed to V_{DDM} and V_{SSM} is unrelated to the array high supply voltage and the array low supply voltage (that is the subject of the Appellant's claim).

The Appellant also respectfully traverses the statements in the Office Action (page 2) that the inherent "voltage drop across the header-diode" and the inherent "voltage drop across the footer-diode" are the advantageously claimed transistor parameter. The Applicant submits that the inherent voltage drop of an SRAM transistor is an inherent response to the transistor parameter, but it is not the transistor parameter. The Applicant notes that the definition of the term "transistor parameter" is defined in

the Specification (paragraphs 0029, 0030, 0031, 0037). Moreover, a statement that "the current leakage is often primarily based on the parameters of the SRAM cell transistors" (page 3 of the Office Action) is not equivalent to the claimed sleep mode voltage controller providing the array high supply voltage and array low supply voltage based on a transistor parameter.

Therefore, Claim 24 is patentable over the patent granted to Deng et al.

Claim 25

Claim 25 is dependent on Claim 24 and is therefore allowable for the same reasons that Claim 24 is allowable. Furthermore, Claim 25 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 24, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 25 further specifies the additional limitation that the sleep mode voltage controller performs the modify based on reducing current leakage of the SRAM array and providing sufficient voltage across the SRAM array via the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} to retain data.

Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach that a sleep mode voltage controller performs the modify based on reducing current leakage of the SRAM array and providing sufficient voltage across the SRAM array via the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS}

to retain data (column 2 lines 48-55). The Appellant respectfully traverses the statement in the Office Action (page 4) that in column 2 lines 24-31 Deng et al. teaches the limitations of Claim 25. Rather, Deng et al. states that an apparatus may "enter the sleep mode while still supplying sufficient voltage across the memory array to retain data", but does not teach that the sleep mode voltage controller has any involvement in modifying the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} or in data retention (column 2 lines 30-31 and 47-55).

Therefore, Claim 25 is patentable over the patent granted to Deng et al.

Claim 26

Claim 26 is dependent on Claim 24 and is therefore allowable for the same reasons that Claim 24 is allowable. Furthermore, Claim 26 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 24, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 26 further specifies the additional limitation that the sleep mode voltage controller provides an array high supply voltage V_{ADD} lower than $V_{n\text{-}well}$ during the sleep mode.

The Office Action is silent as to where Deng et al. teaches that the sleep mode voltage controller provides an array high supply voltage V_{ADD} lower than $V_{n\text{-}well}$ during the sleep mode. Therefore, the USPTO burden under 37 C.F.R. §1.104(c) has not been met. Deng et al. does not teach the advantageously claimed invention because Deng et

al. does not teach that the sleep mode voltage controller provides an array high supply voltage V_{ADD} lower than $V_{n\text{-}well}$ during the sleep mode (column 2 lines 48-55).

Therefore, Claim 26 is patentable over the patent granted to Deng et al.

Claim 27

Claim 27 is dependent on Claim 24, and is therefore allowable for the same reasons that Claim 24 is allowable. Furthermore, Claim 27 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 24, is not taught nor suggested by the patent granted to Deng et al. Namely, Claim 27 further specifies the additional limitation that the sleep mode voltage controller provides the array low supply voltage V_{ASS} higher than a substrate voltage during the sleep mode.

The Appellant respectfully traverses the statement in the Office Action (page 4) that "it is very well known in the art that in any memory integrated circuit the base substrate voltage must be lower than any operating power supply voltage during any operation." The Appellant submits that the lowest operating power supply may be lower than the base substrate voltage in order to provide a forward bias (i.e. to lower Vt's for material at the slow process corner). Therefore, it is incorrect to state that "in any memory integrated circuit the base substrate voltage must be lower than any operating power supply voltage during any operation".

Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach that the sleep mode voltage controller provides the array low supply voltage V_{ASS} higher than a substrate voltage during the sleep mode (column 2 lines 48-53).

Therefore, Claim 27 is patentable over the patent granted to Deng et al.

Claim 28

Claim 28 is dependent on Claim 24, and is therefore allowable for the same reasons that Claim 24 is allowable. Furthermore, Claim 28 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 24, is not taught nor suggested by the patent granted to Deng et al. Namely, Claim 28 further specifies the additional limitation that the sleep mode voltage controller is configured to regulate the array high supply voltage V_{ADD} relative to the array low supply voltage V_{ASS} during the sleep mode.

The Office Action is silent as to where Deng et al. teaches that the sleep mode voltage controller is configured to regulate the array high supply voltage V_{ADD} relative to the array low supply voltage V_{ASS} during the sleep mode. Therefore, the USPTO burden under 37 C.F.R. §1.104(c) has not been met. Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach that the array

high supply voltage V_{ADD} level follows the changes in the array low supply voltage V_{ASS} during the sleep mode (column 2 lines 48-53).

Therefore, Claim 28 is patentable over the patent granted to Deng et al.

Claim 29

Claim 29 is dependent on Claim 24, and is therefore allowable for the same reasons that Claim 24 is allowable. Furthermore, Claim 29 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 24, is not taught nor suggested by the patent granted to Deng et al. Namely, Claim 29 further specifies the additional limitation that the sleep mode voltage controller is configured to regulate the array low supply voltage V_{ASS} relative to the array high supply voltage V_{ADD} during the sleep mode.

The Office Action is silent as to where Deng et al. teaches that the sleep mode voltage controller is configured to regulate the array low supply voltage V_{ASS} relative to array high supply voltage V_{ADD} during the sleep mode. Therefore, the USPTO burden under 37 C.F.R. §1.104(c) has not been met. Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach that the array low supply voltage V_{ADD} level follows the changes in the array high supply voltage V_{ASS} during the sleep mode (column 2 lines 48-53).

Therefore, Claim 29 is patentable over the patent granted to Deng et al.

Claim 30

Independent Claim 30 positively recites that the sleep mode voltage controller concurrently provides the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} to the SRAM array during a sleep mode. These advantageously claimed features are not taught or suggested by the patent granted to Deng et al.

Deng et al. teaches away from the advantageously claimed invention because Deng et al. teaches regulating a high operating voltage V_{DDM} and a low operating voltage V_{SSM} to the SRAM array (column 5 lines 60-63); but Deng et al. does not teach concurrently providing the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} to the SRAM array during a sleep mode (column 2 lines 48-55), as advantageously claimed.

The Appellant respectfully submits that the Office Action arguments incorrectly confuse the array high voltage supply (V_{DDA}) of Deng et al. with the high operating voltage (V_{DDM}) of Deng et al. Similarly, the Office Action arguments incorrectly confuse the array low voltage supply (V_{SSA}) of Deng et al. with the low operating voltage (V_{SSM}) of Deng et al. The Appellant notes that the array high voltage supply is V_{DDA} and the array low supply voltage is V_{SSA} in Deng et al. (column 2 lines 48-55). Therefore, the discussion in the Office Action (pages 2-3) directed to V_{DDM} and V_{SSM} is unrelated to the

array high supply voltage and the array low supply voltage (that is the subject of the Appellant's claim).

Therefore, Claim 30 is patentable over the patent granted to Deng et al.

Claim 31

Claim 31 is dependent on Claim 30 and is therefore allowable for the same reasons that Claim 30 is allowable. Furthermore, Claim 31 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 30, are not taught nor suggested by the patent granted to Deng et al. Namely, Claim 31 further specifies the additional limitation that the sleep mode voltage controller further provides a well voltage and the array high supply voltage V_{ADD}, the array low supply voltage V_{ASS} and the well voltage are provided as a set of optimum values for a general technology class of transistors.

Deng et al. does not teach the advantageously claimed invention because Deng et al. does not teach that a sleep mode voltage controller provides an array high side voltage and an array low side voltage to the SRAM array (column 2 lines 48-53). Rather, Deng et al. teaches that the power-down voltage controller provides a high operating voltage V_{DDM} and a low operating voltage V_{SSM} to the SRAM array (column 5 lines 58-63, column 6 lines 14-34). The Appellant notes that V_{DDM} (cited in the Office

Action) is not the array high supply voltage V_{DDA} plus V_{SSM} (cited in the Office Action) is not the array low supply voltage V_{SSA} in Deng et al. (column 2 lines 48-52).

Therefore, Claim 31 is patentable over the patent granted to Deng et al.

CONCLUSION

For the reasons stated above, the Appellants respectfully contend that each claim is patentable. Therefore, the reversal of all rejections is courteously solicited.

Respectfully submitted,

/Rose Alyssa Keagy/

Rose Alyssa Keagy

Attorney for Appellants

Reg. No. 35,095

Texas Instruments Incorporated

P.O. BOX 655474, M/S 3999

Dallas, TX 75265

972/917-4167

FAX - 972/917-4409/4418

CLAIMS APPENDIX

1. An SRAM device, comprising:

an SRAM array coupled to row peripheral circuitry by a word line and coupled to column peripheral circuitry by bit lines; and

a sleep mode voltage controller configured to provide both an array high supply voltage V_{ADD} that is lower than a high operating voltage V_{DD} and an array low supply voltage V_{ASS} that is higher than a low operating voltage V_{SS} to said SRAM array during a sleep mode;

wherein said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} are provided concurrently and wherein said sleep mode voltage controller provides said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} based on a transistor parameter of at least one transistor of the SRAM array.

2. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller provides said array high supply voltage V_{ADD} relative to a well voltage.

3. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller provides said array low supply voltage V_{ASS} relative to a substrate voltage.

4. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller provides a well voltage at about said high operating voltage V_{DD} during said sleep mode.

6. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller adjusts said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} based on a transistor parameter.

7. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller employs a component selected from the group consisting of:

a transistor,

a diode, and

a low-drop out regulator.

8. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller further provides a well voltage and said array high supply voltage V_{ADD}, said array low supply voltage V_{ASS} and said well voltage are provided as a set of optimum values for a general technology class of transistors.

9. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller adjusts said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} based on a sleep mode current.

10. The SRAM device as recited in Claim 9 wherein said sleep mode voltage controller refines said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} based on a diode leakage current.

11. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller further provides a well voltage such that an n-channel back bias voltage, a p-channel back bias voltage and a voltage across a SRAM cell are all about a same voltage.

12. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller provides said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} based on a minimum voltage across said SRAM array that is sufficient for data retention.

13. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller provides said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} based on a minimum voltage across said SRAM array that is sufficient for data retention and minimizing a total leakage current.

14. A method of operating an SRAM device, comprising:

employing in an integrated circuit an SRAM array coupled to row peripheral circuitry by a word line and coupled to column peripheral circuitry by bit lines; and

providing both an array high supply voltage V_{ADD} that is lower than a high operating voltage V_{DD} and an array low supply voltage V_{ASS} that is higher than a low operating voltage V_{SS} to said SRAM array during a sleep mode;

wherein said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} are provided concurrently and wherein said providing said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} is based on a transistor parameter of at least one transistor of the SRAM array.

15. The method as recited in Claim 14 wherein said providing said array high supply voltage V_{ADD} is relative to a well voltage.

16. The method as recited in Claim 14 further comprising providing a well voltage at about said high operating voltage V_{DD} during said sleep mode.

18. The method as recited in Claim 14 further comprising adjusting said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} based on a transistor parameter.

19. The method as recited in Claim 14 wherein said providing employs a component selected from the group consisting of:

a transistor,

a diode, and

a low-drop out regulator.

20. The method as recited in Claim 14 further comprising providing a well voltage wherein said array high supply voltage V_{ADD}, said array low supply voltage V_{ASS} and said well voltage are provided as a set of optimum values for a general technology class of transistors.

21. The method as recited in Claim 14 further comprising adjusting said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} based on a sleep mode current.

22. The method as recited in Claim 21 further comprising refining said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} based on a diode leakage current.

23. The method as recited in Claim 14 further comprising providing a well voltage such that an n-channel back bias voltage, a p-channel back bias voltage and a voltage across a SRAM cell are all about a same voltage.

24. An SRAM device, comprising:

an SRAM array coupled to row peripheral circuitry by a word line and coupled to column peripheral circuitry by bit lines; and

a sleep mode voltage controller configured to provide both an array high supply voltage V_{ADD} and an array low supply voltage V_{ASS} to said SRAM array during a sleep mode and modify said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} during transition from an active mode to said sleep mode;

wherein said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} are provided concurrently and wherein sleep mode voltage controller provides said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} are based on a transistor parameter of at least one transistor of the SRAM array.

25. The SRAM device as recited in Claim 24 wherein said sleep mode voltage controller performs said modify based on reducing current leakage of said SRAM array and providing sufficient voltage across said SRAM array via said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} to retain data.

26. The SRAM device as recited in Claim 24 wherein said sleep mode voltage controller provides said array high supply voltage V_{ADD} lower than $V_{n\text{-well}}$ during said sleep mode.

27. The SRAM device as recited in Claim 24 wherein said sleep mode voltage controller provides said array low supply voltage V_{ASS} higher than a substrate voltage during said sleep mode.

28. The SRAM device as recited in Claim 24 wherein said sleep mode voltage controller is configured to regulate said array high supply voltage V_{ADD} relative to said array low supply voltage V_{ASS} during said sleep mode.

29. The SRAM device as recited in Claim 24 wherein said sleep mode voltage controller is configured to regulate said array low supply voltage V_{ASS} relative to said array high supply voltage V_{ADD} during said sleep mode.

30. An SRAM device, comprising:

an SRAM array coupled to row peripheral circuitry by a word line and coupled to column peripheral circuitry by bit lines; and

a sleep mode voltage controller configured to provide both an array high supply voltage V_{ADD} that is lower than a high operating voltage V_{DD} and an array low supply voltage V_{ASS} that is higher than a low operating voltage V_{SS} to said SRAM array during a sleep mode;

wherein said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} are provided concurrently.

31. The SRAM device as recited in Claim 30 wherein said sleep mode voltage controller further provides a well voltage and said array high supply voltage V_{ADD}, said array low supply voltage V_{ASS} and said well voltage are provided as a set of optimum values for a general technology class of transistors.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None